

PRN No.	
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PAPER CODE	V315-294B (RE)
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**(AY: 2025-26) December 2025 (ENDSEM) EXAM**  
**TY E&TC (SEMESTER - I) (Pattern 2023)**

**COURSE NAME: System Design using Verilog Branch: E&TC COURSE CODE: ETUA31234B**

**Time: [1Hr 30 Min]**

**[Max. Marks: 40]**

(\*) Instructions to candidates:

- 1) Figures to the right indicate full marks. Use of scientific calculator is allowed.
- 2) Use suitable data wherever required.
- 3) All questions are compulsory. Solve any two sub question each from Questions 1 and 2.
- 4) Solve any one sub question (2 marks) from Questions 3, 4, 5 and 6 and sub question of 4 marks is compulsory from questions 3, 4, 5, and 6.

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) Design a 1-bit full subtractor in Verilog using behavioral modelling.	[4]	CO1	[3]
	b) Design a 1-bit full adder using two half adders and OR gate in Verilog.	[4]	CO1	[3]
	c) Design 8-bit adder using addition operator in Verilog.	[4]	CO1	[3]
Q.2	a) Design D Flip-flop with synchronous Set and Reset inputs in Verilog.	[4]	CO2	[3]
	b) Design an 8-bit UP counter with asynchronous Reset in Verilog.	[4]	CO2	[3]
	c) Design 4-bit shift register to do Right shift operation in Verilog. Use asynchronous clear input to reset the data.	[4]	CO2	[3]
Q.3	a) What would be the output of the following statements? 1. latch = 4'd12; \$display ("The current value of latch = %b", latch); 2. in_reg = 4'd12; \$monitor ("In register value = %b", in_reg[2:0]);	[2]	CO3	[2]
	<b>OR</b>			
	b) What will be the time period of the clock (clk) generated by the following code segment?	[2]	CO3	[2]

	<pre> `timescale 10ns/1ns module test_dut; reg clk initial     #0.35 clk = 1'b0; always     #0.63 clk = ~clk; endmodule </pre>			
	c) Design a positive edge triggered SR Flip-Flop using user defined primitive in Verilog.	[4]	CO3	[3]
Q.4	a) State any four Artix-7 FPGA family features.	[2]	CO4	[1]
	<b>OR</b>			
	b) four any four XC9572 CPLD specifications.	[2]	CO4	[1]
	c) Construct the circuit to implement the following functions using PLA. Use only four product terms. $F_1(A, B, C) = \sum m(0,1,2,4)$ $F_2(A, B, C) = \sum m(0,5,6,7)$	[4]	CO4	[3]
Q.5	a) Draw the flowchart to do multiplication by repeated addition.	[2]	CO5	[2]
	<b>OR</b>			
	b) Draw the flowchart to do GCD computation.	[2]	CO5	[2]
	c) Design 32 x 16 register bank with asynchronous reset in Verilog.	[4]	CO5	[3]
Q.6	a) List the step-wise micro-instructions required to execute instruction ADD R3, R6, R8.	[2]	CO6	[2]
	<b>OR</b>			
	b) List the step-wise micro-instructions required to execute instruction SW R2, 30 (R10).	[2]	CO6	[2]
	c) Construct the pipelined architecture to do the following computations. Write a Verilog code to implement this architecture. $X1 = A * B$ ; $X2 = C + D$ ; $X3 = X1 - X2$ ; $F = X3 * C$	[4]	CO6	[3]